ABSTRACT

Switching Power Converters (SPC) has been widely employed in consumer products. SPCs are commonly controlled by Pulse Width Modulation (PWM) with high switching frequency. Consequently, it has the features of high efficiency and light weight. A small amount of dominated harmonic clusters are shown on the spectrum, because of the constant switching frequency. These dominant harmonic clusters cause Electro-Magnetic Interference (EMI) to other electronic devices through radiated or conducted in nature.

EMI is a significant concern in SPC, because of high-voltage / high-current switching. SPCs should meet the Electro-Magnetic Compatibility (EMC) standards such as Federal Communications Commission (FCC) and Verband Deutscher Elektroniker (VDE). Instead of inserting an EMI filter on the input side of the power converters, numerous random-switching methods have been developed to decrease the Conducted EMI. These noises can never be completely removed but they can be attenuated to altitudes and obey the rules agree to regulatory maximum values.

Conducted EMI has two main resources: (i) effect from reflected ripple current at the input of the converter, (ii) caused by the noise of output voltage switching. Whereas SPCs generate considerable quantity of switching noise, they are besides necessitated to function in EMC responsive appliances. In this case, the device has to persuade, not only electrical characteristics, although EMI regulations, for instance FCC class B or VDE, for the automotive background. The frequency of the Conducted EMI limit is from

450 KHz to 30 MHz for FCC Class B regulations and 150 KHz to 30 MHz for German VDE regulations. Radiated emissions are measured at higher frequencies beyond 30 MHz upto several GHz.

Random PWM (RPWM) techniques have been extensively employed in motor controls. In recent years, related techniques are realized on SPCs to decrease the power of dominant harmonic clusters, in that way decreasing the expenditure of EMI filters. The characteristic of RPWM technique is to spread the dominant harmonic clusters and to decrease the power of dominant harmonic clusters. RPWM methods are categorized into four types: (i) Random Carrier Frequency Modulation with Fixed Duty ratio (RCFMFD), (ii) Random Carrier Frequency Modulation with Variable Duty ratio (RCFMVD), (iii) Random PWM (RPWM), and (iv) Random Pulse Position Modulation (RPPM).

This research work presents a novel RPWM switching technique with constant sampling frequency. Various methods present unvarying sampling frequency, whereas not maintaining constant average inductor current, which effects in the raise of output voltage ripple. A digitally controlled Flyback converter using Field Programmable Gate Array (FPGA) experimental arrangement has been set up. The implementation of the random switching pattern is proposed by XILINX Spartan 3AN. Experimental results make obvious noise reduction of the recommended random switching pattern.

A proportional analysis is presented into the use of various random modulation techniques against the conventional PWM. The effectiveness of randomization on spreading those dominating frequencies that normally exist in constant frequency PWM schemes is evaluated by Power Spectral Density (PSD) estimations in the low-frequency range. Some parasitical and topology based EMI sources in devices are presented and frequency analysis is shown by using Discrete Fourier Transform (DFT).

A spread-spectrum scheme for Conducted noise reduction in Flyback converter uses three randomized parameters to generate the switching signals: carrier frequency, duty ratio and pulse position. The increasing performance and cost reduction of FPGA technology have made the application of these schemes possible in this field. Furthermore, another three different randomization schemes that have not been previously addressed are as follows. (i) Randomized Duty ratio and an RPPM with Fixed Carrier Frequency (RDRPPMFCF), (ii) Randomized Carrier Frequency and RPPM with Fixed Duty ratio (RCFRPPMFD) and (iii) Randomized carrier frequency and a Randomized duty ratio with RPPM (RRRM).

Randomly switched Flyback converter consists of FPGA based digital controller utilizing Analog to Digital Conversion (ADC) circuit, compensator, pseudorandom stream generator and power switching circuit. The converter output voltage is converted into a digital 16-bit signal by means of ADC. This signal is processed by the digital compensator to calculate the duty ratio. Sigma Delta Modulation (SDM) is a type of switching modulation used to reduce the harmonic spikes. The switching frequency is spread by a random dither generator placed on the input side or the output side. The configuration that utilizes the random dither placed at the output side of quantizer in the SDM is called Time Dither SDM (TDSDM).

A random dither is used as a control signal to make the update or maintain changes to its state and thus to decide the switching instants. In TDSDM, the signals are classified by the location of their random dither additions. The output of the time dither is a binary signal, either 0 or 1. When it is 0, the update or maintain block is in the update state and the TDSDM behaves like a SDM. When the value of the time dither is 1, the update or maintain block is changed to the maintain state, and the output value of the TDSDM remains unchanged.

Randomized Pipelined Sigma Delta Modulator (RPSDM) offers high degree of concurrence and approximately linear hardware cost with resolution, and it is easy to be reconfigured to different resolution by adopting different stages. Thus Pipelined modulator is a good one for the last stage conversion. The pipelined modulator consists of a cascade of K stages. Each pipeline stage comprises a Sample and Hold Amplifier (SHA), a low resolution coarse ADC, a Digital to Analog Converter (DAC) and a subtractor. During operation, each stage initially samples and holds the output from the previous stage and is then converted into a digital code by the ADC, which is converted back into an analog representation by the DAC.

The difference between the detained analog signal and the output of the DAC is amplified to give the residue for the next stage. The final output is the combination of each stage through a digital correction circuit. The primary advantage of pipelined modulators is that they provide high throughput rates and occupy small die areas. Due to the use of the extra stage, the noise of the proposed technique is reduced by 66 dBμV. This method is also applicable to different converter topologies such as buck, boost and AC-DC converter with single-phase diode bridge front-end.