ABSTRACT

In the last few decades, the exponential scaling in feature size and increase in processing power have been successfully achieved by conventional lithography-based VLSI technology. However, this trend faces serious challenges due to fundamental physical limits of CMOS technology such as ultra-thin gate oxides, short channel effects, doping fluctuations and increasingly difficult and expensive lithography at nano-scale regimes. It is projected that the scaling process of CMOS technology will end by the channel length of 7 nm. There has been extensive research in recent years at nano-scale to supersede conventional CMOS technology. It is anticipated that these technologies can achieve a density of 10^{12} devices/cm^2 and operate at THz frequencies.

Nanotechnology provides new possibilities for computing due to the unique properties that arise at such reduced feature sizes. Among these new devices, Quantum-dot Cellular Automata (QCA) relies on new physical phenomena (such as Coulombic interactions), and innovative techniques that radically depart from a CMOS-based model. The QCA not only gives a solution at nano-scale, but it also offers a new method of computation and information transformation .Consider the processing features of CMOS systems: some circuits (i.e., logic gates) perform computation, while others (i.e., wires) are used for signal/data transfer and communication. In contrast, computation and communication occurs simultaneously in QCA.

The fundamental QCA logic primitives are the three input majority gate, wire and inverter. Each of these can be considered as a separate QCA locally interconnected structure, where QCA digital architectures are combination of these cellular automata structures. The existing QCA circuit designs are based on only majority gate reduction technique. Further reducing the area as well as complexity, the cell minimization techniques are used in this thesis.

This thesis presents the design and QCA implementation of Digital Circuits. The digital circuits are Logic Gates, Combinational Logic Circuits (CLC) and Sequential Logic Circuits (SLC). The area and complexity are the major issues in the circuit design. These circuits are designed with minimum number of cells by using cell minimization techniques. It provides a significant reduction in the area as well as complexity, than the existing methods. This will also reduce the cost of the circuit. The QCA circuits are simulated by QCADesigner Ver 2.0.3. It is a design and simulation tool for quantum dot cellular automata. The tool is used to determine the functionality of QCA circuits. The simulation based performance analysis of the proposed circuits are tabulated and compared with existing majority gate method.

In CMOS design, the logic circuits are usually implemented using AND and OR gates based on sum of products (SOP) or product of sums (POS) formats. In this QCA technology, the basic combinational circuit is the majority gate with three inputs and hence the sum of products expressions are converted into reduced majority logic. In this thesis, first the logic gates are designed by using the basic QCA gate called Majority gate (MG) or Majority

voter (MV).Then the designed majority gate structures are implemented by QCA cells using cell minimization techniques and simulated by QCADesigner.

Next the logical structures are designed by using Nand-Nor-Inverter (NNI) and And-Or-Inverter (AOI) gates. These are universal gates and are used to eliminate the need of separate NOT gate which require more space as well as introduced delay in realizing the large circuits. These types of gates are often used as a logic resource in array structures such as FPGAs.

The NNI gate is a majority gate with two inverted inputs. It offers the advantage of versatility and ease of implementation of logic functions. The logical characteristics of NNI gates are defined here. The rules and algorithms for NNI gates are proposed in this thesis for easy implementation of different logical structures and functions. The performance analysis of the logical structures are tabulated and compared with majority gate design.

The AOI is a five input QCA gate with embedded AND, OR and INV functions. Hence design rules are proposed in this thesis for easy implementation of AOI gates and logical characteristics of AOI is defined here. The designed logical structures using the AOI gates are compared with the conventional CMOS and majority gate based QCA methodology.

A similar approach of majority gate is applied to Combinational Logic Circuits and Sequential Logic Circuits. The most basic combinational circuits are Arithmetic structures. This thesis proposes design and QCA implementation of different types of arithmetic structures such as Adders,

Subtractors and Multipliers. Algorithms for each arithmetic structure are presented in the thesis. The new design is compared with the previous designs. From the results it is found that there is significant reduction in the area as well as complexity of the circuits.

The design of sequential circuits such as Flip Flops (FF), Shift Registers (SR) and Counters are proposed in this thesis. The sequential circuits are designed by using majority gate. Then the designed circuits are implemented with QCA cells and simulated using QCADesigner. The performance analyses of those circuits are compared according to the complexity, area, and number of clock cycles.

The accomplishment of two key issues like area and complexity provides an excellent starting point for future QCA designs. The QCA circuits can function logically and can be used to implement equivalent versions of CMOS circuits. The resulting designs can be used to build an Arithmetic and Logical Unit (ALU) which can be enhanced to design a nanoprocessor.