ABSTRACT

One of the paramount issues in the field of VLSI design is the rapid increase in power consumption. The need to minimize power consumption became prominent due to the increased demand for high performance portable electronic systems like Personal Digital Assistant, notebook, computer, etc. Every digital system is built with a memory unit in it. Register elements such as latches and flip-flops together with clock network constitute the major power-consuming elements in any design. So the design of power-efficient and high-performance memory elements is necessary. They are in great demand which motivates circuit designers to design low power architecture for both full custom and semi-custom design implementation.

A variety of memory element designs have been proposed for different objectives like increased speed, low power, less layout area, etc, but no design has been developed so far which maintains a proper balance between power consumption, area, and speed. Our goal is to design and develop high-performance power- efficient flip-flops and shift registers with the least area and high speed. The performance is boosted up by incorporating different low power reduction techniques in it. Different power reduction techniques are adopted based on its architectural design of each hierarchical level. The major source of power consumption is identified and the design is modified with respect to it. Here, we propose six different power efficient and high-performance designs of memory elements (three flip-flops and three shift registers).

The first proposed work focuses on the design of a power-efficient dynamic double edge-triggered flip-flop named TCRFF (Transistor Count Reduction Flip-Flop). It features a dynamic design comprising of transmission gate in which total transistor count has greatly reduced without affecting the logic. The design is such that there is a reduction in high capacitive loading and switching activity of internal nodes along with the usage of dual-edge clocking.

With reduced charging and discharging of internal nodes with input signal variations further reduces power consumption. It focuses on dynamic power reduction. It has an average power consumption is 0.057 μw with a delay of 2.23 ns occupying a layout area of 8.409 μm^2. A high performance 4-bit Serial Input Parallel Output Shift register named TCRSR (Transistor Count Reduction Shift Register) is developed out of TCRFF to prove its efficiency. It has occupied an area of 29.15 μm^2 with a delay of 4.03 ns for a power consumption of 156.10 nw.

The main goal of the second work is to reduce static power in TCRFF. Therefore, TCRFF is modified by series stacking technique to form another low power DFF named Series Stacking in Transistor Count Reduction Flip-Flop (S-TCRFF). The sub-threshold leakage current which is one of the major factors of leakage current is minimized using 'Series Stacking' technique. We haven't used stacking in all the series transistors to reduce additional area and delay. The merit in stacking is that there is no need for high threshold voltage devices as in other leakage reduction techniques. S-TCRFF has a power consumption of 0.052 μw and an area of 9.486 μm^2 with a delay of 2.29 ns. Its proficiency is further proved by developing its corresponding shift register named S-TCRSR (Series Stacking in Transistor Count Reduction Shift Register). It has occupied an area of 28.87μm^2 with an average power consumption of 127.3 nw with a delay of 4.07 ns.

Lastly, one more power efficient and high performance 4-bit SIPO shift register named FST in TCRSR (Forced Stacking of Transistors in Transistor Count Reduction Shift Register) has been developed using third proposed flip-flop design named FST in TCRFF (Forced Stacking of Transistors in Transistor Count Reduction Flip-Flop). Another method of stacking called 'Forced Transistor Stacking' (FTS) is adopted in TCRFF design where we stack transistors forcefully in non-critical paths to reduce leakage current. Here, the MOS transistors which are close enough to power rails are modified with FTS technique such that the width of the particular transistor (w) is divided into two transistors of equal width (w/2). FST in TCRFF has a power consumption of 0.049 μw and

an area of 8.19 μm^2 with a delay of 2.321 ns. FST in TCRSR has occupied an area of 28.75 μm^2 with a power-saving of 119.40 nw and a delay of 4.12 ns.

All the designs are simulated at a supply voltage of 1V/500MHz when the input switching activity is 25% in Cadence Virtuoso using 45nm CMOS technology. The performance of the six proposed memory elements (TCRFF, S-TCRFF, FST in TCRFF, TCRSR, S-TCRSR and FST in TCRSR) has been compared with nine recently designed flip-flops and the registers developed out of these flip-flops. Different analyses are conducted and many performance measures such as delay, power consumption, setup time, PDP, EDP, leakage power, etc are calculated and are compared with that of recently proposed designs. Reliability of the proposed designs is verified through Monte–Carlo simulation by comparing the performance of the designs in terms of power and delay under different PVT variations.

The performance of all the designs has been improved through one of the metaheuristic algorithms named Elephant Herding Optimization (EHO) algorithm. It is for the first time that the EHO algorithm is implemented in memory elements. Energy-Delay-Product and Leakage Power are selected as the two fitness functions for the algorithm. The device parametric values obtained through parametric analysis which is done in Cadence ADE XL tool has been optimized by applying EHO algorithm. The optimized performance results have been compared with a few optimization algorithms. The performance indices have been ameliorated by applying this algorithm. Some of the power gating techniques can be clubbed together in the future to redesign the circuit to use in deep submicron technologies without incurring area and delay issues.