# ABSTRACT

Faraday Cup Detectors detect and collect ions in many analytical instruments. Ion Mobility Spectrometer is one such analytical instrument. The current signals coming out of the IMS is very small typically in lower tens of picoampere range. Also, the signal is coupled multiple sources of noise. One important source of noise is the high detector capacitance. A high gain precision transimpedance amplifier is required to amplify those signals.

The signal is required to be amplified with 180 dB transimpedance gain, 5 kHz bandwidth and less than 500 $\mu V_{RMS}$ output voltage noise. This work reports the design, development, fabrication and measurement of transimpedance amplifier to meet these requirements.

Amplifier design was done in two design cycles. In the first design cycle a single stage TIA was designed. The design achieved 170 dB transimpedance gains, 6 kHz bandwidth and 800 $\mu V_{RMS}$ output noise voltage. Several observations were made from the first design cycle to reduce the noise performance.

Important noise contributing elements are the input capacitance at the inverting input of the TIA. Detector capacitance, op-amp common mode and differential mode capacitances, TIA feedback capacitance and printed circuit board parasitic capacitances all contribute to the noise significantly.

Several ways are analysed to improve the noise performance. Noise can be reduced by proper op-amp selection which has low input capacitance and careful layout techniques. Several op-amps were analysed and LTC6268 was chosen as op-amp of choice. It has very low input capacitance. It allows innovative layout to reduce the feedback capacitance. With the help of the LTC6268 the feedback capacitor is altogether not required. This reduces the

input capacitance seen by the TIA considerably.

Large feedback resistor is another source of noise. The design incorporated a two-stage design methodology. Required transimpedance gain r is achieved in two stages. The first stage is a TIA with 250 MΩ transimpedance gain followed by the 4 V/V voltage gain.

To achieve low parasitic capacitance many standard low noise board design practices are incorporated. In addition, high impedance current input path is guarded with rings. This reduces the leakage current flowing though the TIA input and errors at output due to them. A track to ground is run underneath the feedback resistor that shields the electric field from reaching the other end of the feedback resistor pad. This reduces the parasitic capacitance considerably. This enabled the noise reduction substantially. All these changes are incorporated in the second design cycle.

The circuit was designed, simulated, fabricated and measurements are made. Measurement results shows that the amplifier has achieved 178 dB transimpedance gains, more than 10 kHz bandwidth and remarkably low noise voltage of 270 $\mu V_{RMS}$. The achieved noise was close to the theoretical limits achievable. TIA designed in the second design cycle was tested with real IMS. Results confirm that the design properly amplifies the FCD signals.