

ABSTRACT

To investigate several types of heart diseases such as cardiac arrest, arrhythmia (abnormal heartbeat), coronary heart disease, and heart failure, the impression of heart electrical signal, called electrocardiogram (ECG), is popularly used. However, the diagnosis of abnormal ECG characteristics is not easy to carry out direct information retrieval, due to the intricacy and non-linearity of ECG signals from one hand, and the interference or artifact effect of these signals from the other hand. Hence the digital signal processing, especially digital filter is the pertinent tool to enhance the desired signal features and suppress the unwanted noise or artifact components. At present, digital filtering becomes an essential tool in most critical applications such as biomedical engineering, information security, satellite systems, biometric systems, consumer electronics, data analytics, etc. Notably in the field of biomedicine, signal, image, and video processing approaches are broadly used for better treatment and diagnosis.

The electrical or powerline interference, motion artifacts, and the baseline wander (drift), and radio (high) frequencies are the major noise components are often contaminated with the recorded ECG signal. The central issue in recording electrocardiograms (ECGs) is the existence of power-line interference (either 50 Hz or 60 Hz) because of primarily the instruments' immature connection setup. Naturally, because of body movements, electrode impedance effects, and respiration impacts, baseline wander noise would appear; hence, filtering is essential to extract the intelligence from an ECG signal. But there are more challenges in such applications, for example, filtering muscle noise would be extremely tough as its content overlaps at the same time with an ECG signal during data acquisition from the patient.

The main objective of this research is to implement the widely used digital filters, especially on high-frequency noise and baseline wander removal from the ECG signal, on a field-programmable gate device (FPGA) device. For

better performance results, digital filters would occupy more computational resources and hence consume a larger area, dissipate more power consumption, etc. The primary concern in such hardware designs is the trade-off. For instance, the design may save space, but at the cost of reduced performance, the design may perform better at the expense of higher power consumption.

To remove the high-frequency noise components, several filter design structures of moving average filter are explored. Furthermore, with the reduced hardware structure, the exponential averager is demonstrated for the same purpose (high-frequency noise removal) with the different filter structures. At last, the baseline wander noise removal is achieved using high-speed IIR filters with different styles. The pipelining technique, the widely used method to reduce the critical path delay, is combined with look-ahead transformation and clustered look-ahead transformation for better performance results. The device utilization reports and the power dissipation results are too be detailed in each case. Depends on the demand in real-time application, either to save area or to perform better, the designers can choose the appropriate one.