ABSTRACT

Network on Chip (NoC) is an on-chip scalable medium in a larger area networks and consists of routers, processing elements and Network Interface. The data transmission and reception is possible through the router device in NoC. Router is used to transfer the packets between two or more different network topologies. The microprocessors or Digital signal processors are inbuilt in router device which performs the controlling functions of the data transmission and reception. Generally, all the routers in the network keeps a routing table which contains the address of all other routers presented in the network. The router receives the packet from the other router and strips the destination address from it. The extracted destination address is compared with its routing table to route the incoming packets to its corresponding destination address.

The main problem of the conventional router is its speed limitations and high power consumption due to its requirement of huge memory elements to store the routing table. This research work aims to design a low power and low latency router for larger area NoC architectures. In order to address this problem this thesis is organized with three research works. First one is Multi port encoder based router. Second research work is based on Shared Buffer Router Architecture and third one is Hybrid wire and wireless router scheme.

The First research work proposed is multi port encoding based router architecture. The multiport encoder encodes the incoming packet using processing elements. The cross bar architecture forwards packets either serial mode or parallel mode based on the control bits of the incoming packet. The packets are forwarded towards the output port of the router based on the maximum bandwidth. The port weight based routing methodology of eight

port router is also proposed in this research to reduce the power consumption and increasing the throughput of the system.

In conventional router design, each port of the router has an individual buffer unit for passing the packets towards the router and outwards from the router. The memory consumption of this type of router is high due to these high buffer requirements in each port of the router. Hence, the second research work proposes a new router architecture which has an inbuilt shared buffer among all the ports in router of NoC. The shared buffer is employed between the multi ports of the router architecture. The performance of the proposed router is analyzed in terms of power and current consumption with conventional methods.

The conventional methods for on-chip wireless communication are optical interconnections, RF Interconnect (RF-I) transmission lines. The main limitations of on-chip optical interconnections are that it requires separate transmitter and receiver components, integration of on-chip photonic components which increases the power consumption. RF-I requires additional, physically overlaid transmission lines which serve as wave guides to enable data communication which increases latency of the transmission. The conventional NoC system is based on either wired or wireless topology. The proposed system is based on hybrid of the wired and wireless NoC system, which increases the efficiency of the system. Hence, in the third research work, a hybrid wireless on chip communication interface is proposed to reduce both latency and power consumption. Wireless links are inserted between subnets to form express communication links by replacing baseline wired routers with routers having wireless communication capabilities. The average packet latency and normalized power consumption of proposed hybrid NoC router are analyzed for synthetic traffic loads as shuffle traffic, bitcomp traffic, transpose traffic and bitrev traffic.

In this thesis, the proposed NoC is designed using verilog HDL and simulated using Modelsim software. Xilinx Project Navigator 12.1 is used in this research work for synthesis purposes. The performance of the proposed router in NoC is analyzed in terms of latency, memory requirements, power and current consumption with conventional methods.