ABSTRACT

The multiplier indeed constitutes a critical operation block within any processing unit, dictating the speed and efficiency of arithmetic computations. Among the plethora of multiplication algorithms available, the Wallace tree multiplication algorithm stands out for its advantageous speed of operation. As technology advances, there is a growing demand for circuits that deliver high-speed performance while minimizing area utilization. To address this demand, a novel structure for the Wallace tree multiplier is proposed in this paper. The primary objective is to enhance the speed of operation without compromising on the area parameter. In the proposed structure, a crucial enhancement lies in the final addition stage of partial products, where a Carry Lookahead Adder (RDCLA) is employed. Carry Lookahead Adders are renowned for their ability to expedite addition operations by concurrently computing carry signals across multiple stages, thereby mitigating the inherent delay associated with carry propagation in conventional adders. By integrating a RDCLA into the final addition stage of the Wallace tree multiplier, the overall speed of the multiplication process is significantly improved. Furthermore, to validate the effectiveness of the proposed structure, multiplier structures are meticulously designed using Verilog Hardware Description Language (HDL) within the Xilinx Design Suite. This facilitates the simulation, synthesis, and implementation of the proposed architecture, enabling a comprehensive evaluation of its performance metrics, including speed and area efficiency.

In summary, the proposed enhancement to the Wallace tree multiplier, utilizing a Carry Lookahead Adder in the final addition stage, offers a promising avenue for achieving high-speed multiplication operations while maintaining optimal area utilization. The adoption of Verilog HDL and the Xilinx Design Suite ensures rigorous evaluation and validation of the proposed architecture, paving the way for advancements in high-performance computing applications.