

ABSTRACT

Finite Impulse Response (FIR) filters are essential components in digital signal processing (DSP) for tasks such as signal smoothing, noise reduction, and frequency filtering. FIR filters process input signals to produce desired output signals based on a set of filter coefficients. These filters are known for their stability and linear phase response, making them a popular choice in many applications. This project optimizes FIR filters for DSP tasks by using Wallace Tree multipliers and approximate adders. Designed in Verilog language and implemented with Xilinx Vivado tools, this method yields promising results for low-voltage, low-power VLSI applications. Wallace Tree multipliers accelerate multiplication between input samples and filter coefficients, while approximate adders boost computational efficiency by permitting minor inaccuracies, which are tolerable in many DSP applications. This combination achieves optimal area utilization and reduces the silicon footprint. Additionally, the design minimizes power consumption upto 62% and 70% improvement in area utilization. This approach offers a significant advancement in the performance and efficiency of FIR filters for various DSP tasks.