ABSTRACT

Reconfigurable array processors have proven to be an effective solution for speeding up computationally heavy applications. As the frequency of memory access increases, they may experience a data access bottleneck. The distributed cache design of the reconfigurable array processor currently has a high cache failure rate, and frequent access to external memory results in significant memory access delays. To address this issue, we propose a Runtime Dynamically Migration Mechanism (RDMM) of distributed cache for reconfigurable array processors that is based on obvious locality and high parallelism in data accessing. This approach enables the dynamic migration of temporary, static data from the remote cache to the processor's local migration storage table dependent on how frequently the reconfigurable array processors access the remote cache. By using a data search method based on migrating storage tables, we can reliably acquire the data on the shortest path, thereby minimizing the system's access delay and boosting the memory bandwidth of the reconfigurable array processor. To test the proposed approach, we use the reconfigurable array processor hardware platform. The ability to move and defragment setups on an FPGA can significantly reduce the overall reconfiguration overhead caused by reconfigurable technology. As a result, we describe hardware solutions for providing relocation and defragmentation support with minimal area increase compared to a generic partially reconfigurable FPGA, as well as software algorithms for managing this hardware. The configuration overheads of standard serially programmed FPGAs are reduced by factors of 8 to 12 as a result.